

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	2472	(stack\$3 near3 gate) with (sidewall side near3 wall spacer lining liner)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/06/01 13:21
L4	1876	3 and ((etch\$3 remov\$3) with (sidewall side near3 wall spacer lining liner))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/06/01 13:22
L5	715	4 and (bitline bit adj line)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/06/01 13:23
L6	605	5 and ((dielectric insulat\$3) with (opening trench hole contact via))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/06/01 13:24
L7	56	6 and ((etch\$3 remov\$3) with (partial\$2 with expos\$3))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/06/01 13:40
L8	1	"6365497".PN.	USPAT; USOCR	OR	ON	2005/06/01 13:32
L9	1	"6168984".PN.	USPAT; USOCR	OR	ON	2005/06/01 13:35
L10	1	"6127260".PN.	USPAT; USOCR	OR	ON	2005/06/01 13:35
L11	1	"6117725".PN.	USPAT; USOCR	OR	ON	2005/06/01 13:36
L12	1	"6069038".PN.	USPAT; USOCR	OR	ON	2005/06/01 13:36
L13	1	"6069038".PN.	USPAT; USOCR	OR	ON	2005/06/01 13:37
L14	164	6 and ((etch\$3 remov\$3) with (partial\$2 ))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/06/01 13:40
L15	79	6 and ((liner lining sidewall side adj wall) with (partial\$2 ))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/06/01 13:40

S16	2166	(stack\$3 near3 gate) with (sidewall side near3 wall spacer)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/01/03 07:31
S17	2188	(stack\$3 near3 gate) with (sidewall side near3 wall spacer linning liner)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/06/01 13:21
S18	1606	S17 and (etch\$3 with (sidewall side near3 wall spacer linning liner))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/06/01 13:22
S19	1364	S17 and silicide	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/12/27 12:52
S20	511	S19 and (bitline bit adj line)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/06/01 13:23
S21	441	S20 and ((dielectric insulat\$3) with (opening trench hole contact via))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/06/01 13:24
S22	319	S21 and (etch\$3 with (partial\$2 wiht expos\$3))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/06/01 13:25
S23	319	S22 and gate	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/12/27 12:57
S24	317	S23 and substrate	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/12/27 13:08
S25	195	S24 and (gate with cap\$4)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/12/27 13:09
S26	1	"6066541".PN.	USPAT; USOCR	OR	ON	2004/12/27 16:20
S27	1	"6043529".PN.	USPAT; USOCR	OR	ON	2004/12/27 16:20

S28	1	"5989952".PN.	USPAT; USOCR	OR	ON	2004/12/27 16:20
S29	1	"5972747".PN.	USPAT; USOCR	OR	ON	2004/12/27 16:20
S30	1	"5929526".PN.	USPAT; USOCR	OR	ON	2004/12/27 16:20
S31	1	"6136651".PN.	USPAT; USOCR	OR	ON	2004/12/27 16:31
S32	1	"5998262".PN.	USPAT; USOCR	OR	ON	2004/12/27 16:31
S33	9	10/038845	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/12/28 16:33
S34	0	"10899024"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/12/28 16:33
S35	0	"10/899024"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/12/28 16:35
S36	1	"6835966"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/12/28 16:51
S37	0	10/899024	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/12/28 16:36
S38	7	"6580098"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/12/28 16:52
S39	45	"6121121"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/12/28 16:52
S40	1	"6365921".PN.	USPAT; USOCR	OR	ON	2004/12/28 17:28
S41	1	"6355497".PN.	USPAT; USOCR	OR	ON	2004/12/28 17:28

S42	1	"6146457".PN.	USPAT; USOCR	OR	ON	2004/12/28 17:28
S43	1	"6121121".PN.	USPAT; USOCR	OR	ON	2004/12/28 17:28
S44	1	"6380108".PN.	USPAT; USOCR	OR	ON	2004/12/28 18:26
S45	1	10/654449	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/01/03 07:31



L12: (1) "6069038".PN.  
 L13: (1) "6069038".PN.  
 L14: (164) 6 and ((etch\$3 remov\$3) with (partial\$2 ))  
 L15: (79) 6 and ((liner lining sidewall side adj wall) with (partial\$2 ))  
 L16: (568) 6 and ((liner lining sidewall side adj wall) with- (partial\$2 ))  
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 = 6 and ((etch\$3 remov\$3) with (partial\$2 with excep\$3))

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6 and ((liner lining sidewall side adj wall) with (partial\$2 ))

M. PCPUE M. KARPEN   Yes  Return

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45	r	r	US 6723623	2004042	15	Methods of forming impl	438/525	257/E21.6		Nguyen; Phong N.	r	r	r	r	r	r																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	</

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6 and ((liner lining sidewall side adj wall) with (partial\$2 ))

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	U	Document I	Issue Dat	Page	Title	Current O	Current X	Retrieval	Inventor	S	C	P	2	3
26	r	US 2002010	2002080	14	Dual work function semic	257/10	257/261;		Ye, Qiuyi et al.	r	r	r	r	r
27	r	US 2002007	2002061	22	Method of enhancing adh	438/629	257/E21.2		Gilbert, Stephen R.	r	r	r	r	r
28	r	US 2002006	2002053	17	Passivation of sidewalls o	257/344	257/E21.2		Pan, Pai-Hung et al.	r	r	r	r	r
29	r	US 2002005	2002051	14	METHOD FOR MANUF	438/241	257/E21.6		Hong, Suk-Gu et al.	r	r	r	r	r
30	r	US 2002000	2002012	25	High performance, low p	257/330	257/E21.6		Arnacost, Michael	r	r	r	r	r
31	r	US 2002000	2002011	21	Hydrogen-free contact et	438/3	257/E21.0		Ma, Shawning et al	r	r	r	r	r
32	r	US 2001004	2001112	22	Method of planarizing a c	438/653	257/E21.3		Gilbert, Stephen R.	r	r	r	r	r
33	r	US 2001003	2001102	22	Hardmask designs for dry	438/396	257/E21.0		Moise, Theodore et	r	r	r	r	r
34	r	US 2001000	2001060	25	HIGH PERFORMANCE	257/327	257/E21.6		ARMACOST, MIC	r	r	r	r	r
35	r	US 6897145	2005052	24	Method for fabricating se	438/637	438/250;		Park, Je-Min	r	r	r	r	r
36	r	US 6878991	2005041	26	Vertical device 4F2 EEP	257/328	257/316;		Forbes, Leonard	r	r	r	r	r
37	r	US 6872640	2005032	20	SOI CMOS device with r	438/514	257/347;		Mouli, Chandra V.	r	r	r	r	r
38	r	US 6844591	2005011	24	Method of forming DRA	257/330	257/332		Tran, Luan C.	r	r	r	r	r
39	r	US 6815290	2004110	17	Stacked gate flash memor	438/257	438/259;		Lin, Chi-Hui et al.	r	r	r	r	r
40	r	US 6806187	2004101	17	Electrical contact for hig	438/675	438/240;		Graettinger, Thoma	r	r	r	r	r
41	r	US 6768164	2004072	17	Stacked gate flash memor	257/321	257/401;		Lin, Chi-Hui et al.	r	r	r	r	r
42	r	US 6767789	2004072	30	Method for interconnecti	438/254	257/306;		Bronner, Gary B. et	r	r	r	r	r
43	r	US 6744089	2004060	23	Self-aligned lateral-transi	257/301	257/296;		Wu, Ching-Yuan	r	r	r	r	r

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